Intel Developer Update is Intel's monthly online news magazine for developers. As the official publication of developer.intel.com, it brings hardware, software, and Web developers the latest information on Intel initiatives, technologies, platforms, and products.

Cover Story

Each month, we run a cover story on the most significant industry announcement, trend, or development for the month.

Featured Articles

Delivering in-depth reports on key platforms, products and technologies, our featured articles provide a monthly source of information on issues affecting developers. Be sure to check in every month for the latest developments driving the evolution of the industry.

Contact the Editor

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Archives

Our archives contain two groups of previously published articles. One group contains all the articles that appeared in *Platform Solutions News*, the earlier version of *Intel Developer Update*. The articles date from September 1997 through August 1999. The other group is set up to contain *Intel Developer Update* articles dating from the inaugural September/October 1999 issue.

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Cover Story

Putting it All Together: Intel's "Wireless-Internet-on-a-Chip"

Al Fazio
Principal Engineer
Intel Technology and Manufacturing Group
Intel Corporation

Overview

Advances in chip-level integration have driven ongoing improvements in the size, performance, power consumption, and cost of wireless communications and computing devices. Until now the computing, memory subsystems, and analog communications of wireless products have involved separate chips with separate manufacturing processes. Developers must also contend with battery life limitations, which have compromised the ability of wireless devices to support rich Internet applications at the heart of the data-voice convergence, including video media. At the Intel Developer Forum (IDF) Conference Spring 2001 in Amsterdam, Intel announced an innovative process technology designed to solve these problems by integrating computing, communications, and memory subsystems on a single chip.

By merging Intel's leading-edge low-power, high-performance logic technology with Intel's high-density flash memory technology, and adding precision analog elements, Intel is able to cost-effectively integrate all the key silicon technology elements required for the next generation of wireless devices–without compromising performance or density. This new wireless-Internet-on-a-chip integration provides a platform for the development of new generations of Internet access devices with broadly expanded capabilities, increased processing power, and significantly extended battery life.

Intel process technologists have overcome the complexities associated with the traditionally separate optimization paths for flash, logic, and analog manufacturing processes. The resulting wireless-Internet-on-a-chip technology utilizes one process to integrate all three functions on a single silicon wafer.

The first of Intel's wireless-Internet-on-a-chip products will integrate the Intel® XScale™ microarchitecture core, Intel® Micro Signal Architecture baseband core, flash memory cores, and embedded SRAM cores, and will be manufactured on Intel's 0.13µ silicon process technology. Processor cores developed with the new technology are capable of operating at clock speeds of up to 1 GHz and providing extended battery life. Initial versions of the chip are scheduled to enter production during 2002.

A New Wireless Generation

Consumer demand for greater flexibility and richer content is driving the convergence of communications and computing in wireless devices. To meet these requirements, the industry is focusing on the development of a new generation of Internet-enabled wireless products including third-generation (3G) cell phones, two-way pagers, automotive navigation and communication systems, and increasingly sophisticated handheld computers and PDAs.

Going forward, wireless devices may feature a variety of processor-intensive signal processing capabilities such as speech and handwriting recognition, text-to-speech translation, and color displays with full-motion video.

At the same time, there has been a dramatic increase in the amount of data available to wireless client devices, due to the emergence of DSL and cable modems and connectivity technologies including the Bluetooth* specification, GPRS (General Packet Radio Service), and 3G cellular technology.

In most current wireless designs it is necessary to conserve chip and board real estate while extending battery life. Designing to save power and real estate often involves trade-offs in computational performance, application flexibility, and functionality. For example, the CPU is often required to handle some DSP functions for communications control in addition to its primary function of application processing. The alternative in current designs is to implement separate core subsystems for the CPU, baseband circuitry, and memory, requiring the complex integration of multiple chips or chipsets.

Physical Integration with Architectural Decoupling

While Intel has integrated wireless subsystems at the physical level, it is important to recognize that single-chip integration continues to support decoupling of the computing function from the communications stack at the architectural level, as defined by the Intel® Personal Internet Client Architecture (Intel® PCA).

Intel PCA is a system-level architecture designed to accelerate the development of applications and hardware for next-generation wireless Internet devices. In addition to speeding time-to-market, Intel PCA supports multiple operating systems and wireless air interfaces to enable easy portability and scalability across multiple market segments and geographies.

Intel PCA speeds development by breaking down the traditional wireless development environment into functional subsystems for computation, baseband communications, and memory:

- *Computation*: Intel XScale microarchitecture, the industry's most highly scalable low-power architecture, is capable of delivering the highest available MIPS/mW performance.
- *Communications*: Baseband circuitry with Intel Micro Signal Architecture, a highly integrated DSP architecture developed by Intel and Analog Devices, Inc. (ADI), provides microcontroller functionality for high performance in battery-powered communications applications.
- *Memory*: Intel® flash memory, the densest flash memory in the industry, combining greater capacity with high performance and lower power consumption.

Decoupling the compute and communication functions at the architectural level separates the development of computing applications from communication standards and makes it possible to dedicate resources to each major function in ways that achieve greater performance and functionality. Intel PCA also describes open application programming interfaces and services between communication and application software, which adds greater design flexibility to meet the requirements of a variety of different applications.

With the independent software development architecture supported by Intel PCA, application developers can rely on the wireless-Internet-on-a-chip to provide the hardware platform, including computational, DSP, and memory resources required for rich multimedia and data-centric applications.

New Process Technology

Traditionally, flash and logic technologies have been developed and manufactured on separate wafers, separate manufacturing equipment, and separate fabrication facilities. As a result, when integration of the two technologies has occurred, significant compromises were needed in logic transistor performance, flash memory density, or both.

During 0.25µ flash technology development, in the 1997 time frame, Intel made a strategic decision to develop the process technology synergistically with 0.25µ high-performance logic technology. This was done to ensure the manufacturing equipment and fabrication facilities could be shared between the two, allowing Intel to more flexibly apply its manufacturing capacity to meet dynamic market demands. The synergistic development initiated the learning required to overcome the historic separate optimizations required of the two technologies.

Wireless-Internet-on-a-chip technology represents the final, complete merging of the two technologies without compromising performance or density. Additionally, precision analog features are added for complete system-on-a-chip capabilities. The analog features are simple add-ons to the flash/logic base technology. Now, the three functions have all been integrated onto the same wafer using the same manufacturing process steps in the same facility.

Integrating the three subsystems on a single chip yields a variety of advantages:

- Integration of many components into fewer components saves space, which provides an opportunity for OEM manufacturers to create a smaller, lighter device or a device with more features at the same size.
- The merging of the memory with the processor provides for faster memory access over a wider data bus. This improved memory access greatly enhances overall processor performance. Higher levels of performance are now achievable, allowing for new applications and features to be developed.
- The elimination of external buses (and bus drivers), previously required in chip-to-chip communication, reduces power consumption.
- Fewer discrete components improve overall system reliability.

Feasibility test studies of the wireless-Internet-on-a-chip process were accomplished at 0.18µ. Products will be developed at 0.13µ and will ultimately scale to a gate width of 0.07µ and beyond. The new wireless-Internet-on-a-chip process technology will be deployed in several Intel fabrication facilities around the world.

Important Benefits

Intel plans to move all future wireless products to the new process technology. The modularity of the process technology provides a platform technology that can be used to allocate logic, analog, and flash memory resources in a variety of combinations to flexibly meet the specialized requirements of a wide spectrum of wireless applications.

- *Intel® logic process technology* has been used to create the fastest transistor used in volume production. It provides industry-leading transistor performance at low operating voltage, which holds the key to low power and superior battery operation.
- *Intel XScale Microarchitecture* features Intel® Dynamic Voltage Management that enables on-the-fly scaling of core frequency and voltage so applications can utilize the right blend of performance and power consumption and deliver industry-leading MIPS/mW capability. Intel® Media Processing Technology features a multiply-accumulate coprocessor (MAC) capable of performing two simultaneous 16-bit SIMD multiplies with 40-bit accumulation for efficient media processing.
- *Intel flash memory* features the smallest NOR-based flash memory based on the most advanced photolithography in the industry. Intel® StrataFlash™ memory incorporates multilevel cell technology to store more than one logical bit in each physical memory cell. This technology has contributed to a 200-fold increase in flash memory density since 1986. The wireless-Internet-on-a-chip technology is capable of supporting multilevel cell Intel StrataFlash technology in addition to one-bit-per-cell density.

Summary

Intel has achieved a significant milestone in semiconductor manufacturing by developing a process technology that combines the core components found in today's cellular telephones and handheld computers on a single silicon chip. This highly integrated wireless-Internet-on-a-chip is designed to drive a new era of wireless connectivity characterized by higher performance and greatly extended battery life. Currently executed with Intel's 0.13µ process technology, the new technology will be capable of operating at 1 GHz and significantly extend battery life.

Intel's new highly integrated chip provides a hardware platform for Intel PCA, an architecture that defines computation, storage, features, interfaces, and peripherals across a broad range of wireless platforms. It supports common capabilities and connectivity that enable application compatibility, scalability, peripheral expansion, and device modularity.

Intel developers expect the wireless-Internet-on-a-chip to bring to reality a wide range of application-rich wireless devices and applications, including wearable computing and communications appliances, wireless devices with video displays, multifunction PDAs with voice-activated calendars, remote health monitors, and inexpensive "disposable" phones.

By applying its core competencies in process technology, Intel continues to achieve the industry's highest levels of integration and low-power performance, combining leading-edge logic, flash, and analog silicon technologies.

More Info

For an overview of Intel process technology, including scaling to 0.13µ and beyond, visit Intel's Silicon Showcase Web site.

Check out the Intel Personal Internet Client Architecture site for a white paper, technical brief, and other information on accelerating hardware and software development for next-generation personal Internet clients.

For information on Intel XScale microarchitecture, including a technical summary, product brief, and benchmark data, visit the Intel XScale Microarchitecture Web site.

Intel and Analog Devices maintain a DSP Joint Development Site with detailed information on Intel Micro Signal Architecture. Also see the cover story, *Micro Signal Architecture: More than a DSP*, in the January 2001 issue of Intel Developer Update.

Comprehensive information on Intel StrataFlash memory is available on the Intel Flash Memory Web site.

Author Bio

Al Fazio is a principal engineer in Intel's Technology and Manufacturing Group. He received his B.S. in physics from the State University of New York at Stony Brook in 1982 and joined Intel the same year. He has worked on numerous technology development programs such as SRAM, EPROM, E2PROM, NVRAM, and Flash memories and was responsible for the silicon process technology development of the Intel StrataFlash memory. Al holds more than 20 patents covering a wide range of technical topics, and he has authored or co-authored several technical papers, two of which have won outstanding paper awards at IEEE-sponsored conferences. He has previously served as general chairman of the IEEE Non-Volatile Semiconductor Memory Workshop.

Column

From the Editor
Donna Loveland
Managing Editor
Intel Developer Update Magazine
Intel Corporation

Column

At May's Intel Developer Forum Conference in Amsterdam, Intel unveiled an experimental chip that could revolutionize Internet access. The subject of this month's cover story, "wireless-Internet-on-a-chip," involves a new process technology that combines the core components of cellular phones and handheld computers. A new era of wireless Internet-access products with longer battery life and greater processing power could be on the way.

Evidence of the converging evolution of computing and communications is already visible in sports immersion, where traditional television content is digitally enriched and delivered to consumers over the Internet. You'll find a snapshot of the latest in event modeling and detection technologies for developers.

IDU also examines the new SDK for the Intel® IXP1200 Network Processor family. Its newly announced development environment is aimed at accelerating the implementation of new services in network equipment. USB 2.0 and audio technology likewise forge ahead, as evidenced by their renewed presence in on-board products.

Here's the article roster for this month:

Putting it All Together: Intel's "Wireless-Internet-on-a-Chip"–cover story–Intel has developed a process technology that combines the core components of cellular telephones and handheld computers on a single chip. This highly integrated chip is designed to drive wireless connectivity characterized by higher performance and greatly extended battery life.

Delivering Immersive Soccer Content to Sports Fans–Intel's cutting-edge technologies for 3D sports immersion event modeling and event detection let developers give users on-demand, customized, and personalized video highlights, instant replays, immersive viewing, player statistics, active links, and more.

A Comprehensive Programming Environment for Intel® IXP1200–With the Intel® Internet Exchange Architecture Software Developers Kit version 2.0 for the Intel® IXP1200 Network Processor, Intel introduces a total programming environment for simplifying and accelerating development of IXP1200 processor-based designs.

Intel® Desktop Boards Support USB 2.0 Standard–Intel is committed to supporting the USB 2.0 standard in all its future desktop board families. Product support includes a discrete controller on motherboards; industry support includes ongoing work through the USB-IF spec development and plugfest activities.

SoundMAX* with SPX and Enhanced Audio–Intel offers PC integrators exceptional audio features with its new on-board audio solution. SoundMAX* with SPX provides enhanced value without consuming PCI expansion slots. Its cost is typical of traditional integrated audio solutions.

In the coming months, Intel Developer Update will keep you close to the latest news coming out of IDF Conferences and the industry advances they present to the worldwide developer community.

Enjoy.

Author Bio

Donna Loveland is the editor of Intel Developer Update magazine. She joined Intel's Technology and Initiatives Marketing group in 1999 as the editor of Platform Solutions News. Donna began her career with Intel in 1982 as a technical editor in an advanced microprocessor development group. Since then, she's held communications positions in leading-edge technology areas ranging from stereoscopic display to digital broadcast to scalable online content. Donna has a B.A. degree in English from the University of Rochester and an M.A. in expository writing from the University of Iowa.

Departments

Desktop

SoundMAX* with SPX and Enhanced Audio

Christine McMonigal
Senior Product Marketing Engineer
Desktop Platform Solutions Division Marketing
Intel Corporation

Overview

There's good news for Intel® Desktop Board customers, including PC OEMs and system integrators. Now users can enjoy a truly robust, consumer grade audio solution integrated on the motherboard. This solution includes uniquely powerful real-time sound production capabilities and an audio bundle and will be offered exclusively on Intel Desktop Boards for at least six months.

The integrated audio solution, SoundMAX* with SPX, is provided by Analog Devices, Inc. (ADI). The solution includes an ADI audio converter (CODEC) and SoundMAX software drivers. It delivers digital sound quality to PC users equivalent to what they expect from high end consumer audio equipment. SoundMAX ensures high-fidelity recording and playback of popular audio format, including MP3, streaming audio, 3D multiplayer gaming, and Web conferencing.

SoundMAX offers unprecedented Audio Animation through Sound Production Extensions (SPX). These extensions create sound in real time for a remarkable level of realism and responsiveness. The solution provides enhanced value without having to consume any PCI expansion slots. The cost is typical of traditional integrated audio solutions.

Enhanced Value for Integrators

In addition to SoundMAX, Intel is also providing integrators with a software audio bundle to complement their system sales. The software bundle includes NTI CD-Maker* 2000 (for creating audio and data CDs), RealPlayer* Basic (for Internet streaming media), and RealJukebox* (for recording and listening to MP3 audio).

SoundMAX marks a departure from what integrators traditionally have done to make audio available on their systems. For most business-oriented systems, integrators have deployed audio on the motherboard, but those solutions have been fairly simple in terms of capabilities and not particularly robust. For mainstream consumer and high end systems, integrators have installed PCI-based add-in cards such as SoundBlaster*. But add-in cards carry a much higher price tag than integrated audio solutions. They can also introduce potential conflicts with software and require added labor for installation and testing.

Having the audio solution with SoundMAX on the motherboard changes all this. Now, integrators have a fully functional and highly robust solution with capabilities largely matching, and in some areas easily exceeding, those of the typical add-in card. Even for integrators serving a customer base requiring more than two channels, a multi-channel solution can be easier to implement and more affordable than traditional approaches. Intel Desktop Boards with integrated ADI audio can easily be upgraded with a CNR-based add-in card that provides 6-channel audio.

SoundMAX will change the way integrators implement PC audio–and the way they think about it. Until now, integrated audio was often unsuitable for needs beyond those of the basic business user. With SoundMAX and its uniquely interactive audio synthesis and processing capabilities, its support for multi-channel surround sound, its 3D spatialization and environmental effects, and its uniform device driver, integrated audio can now appeal to enthusiasts. SoundMAX is generating considerable interest and excitement throughout the industry.

Shipping Began May 2001

SoundMAX with SPX is the third release of the SoundMAX integrated audio solution from Analog Devices. Intel has worked closely with ADI since early 2000, when it shipped SoundMAX versions 1.0 and 2.0 on D815EEA, D815EFV, D815EEA2, D850GB, and D810E2CA3–all to highly favorable reviews.

Intel began shipping SoundMAX with SPX, including the enhanced audio bundle consisting of NTI CD-Maker 2000, RealPlayer, and RealJukebox, on the new configurations of D815EFV and D815EEA2 with universal support for Intel socket-370 processors, followed by D850GB. SoundMAX with SPX will be offered exclusively on Intel Desktop Boards for at least six months.

Integrators will have their choice of audio driver configurations. If storage space is a concern, they can use the driver-only configuration (5 MB). If they wish to exploit SoundMAX with SPX to its fullest potential, they can use the SoundMAX with SPX driver (34 MB). Both drivers ship on the driver CD-ROM included with Intel Desktop Boards and are available for download from the Intel Developer Web site.

Summary

SoundMAX with SPX provides integrators an affordable way to provide mid-to-high-end audio–including a powerful animated audio capability that's available in no other solution, either integrated or add-in–for less cost and effort than what's required to install and support add-in cards. SoundMAX with SPX delivers a strong competitive advantage to integrators building systems with Intel Desktop Boards.

Along with integrators, users will benefit from the availability of SoundMAX with SPX on Intel Desktop Boards. For a price close to what they've been paying for systems with integrated audio–or less than what they've paid for systems relying on add-in cards–users can enjoy an unparalleled PC audio environment for business, home, recreational, and educational activities.

More Info

For more information on how SoundMAX with SPX will be integrated with the various Intel Desktop Boards, go to the Intel Desktop Boards Web site. Click on Driver Upgrades, then select one of the following Intel Desktop Boards: D815EEA2 / D815EPEA2, D815EFV / D815EPFV, D850GB.

For more technical detail on SoundMAX with SPX, visit the Analog Devices Web site.

Other information is available through the author of this article, Christine McMonigal.

Author Bio

Christine McMonigal is a senior product marketing engineer in Intel Desktop Platform Solutions Division (DPSD) Marketing, where she defines features for new desktop boards and markets them to customers. She has eight years of experience in the computing industry as well as an M.B.A. from Cornell University. Before joining Intel in 2000, she was the reseller marketing manager for a manufacturer of networking and communications hardware.

Intel® Desktop Boards Support USB 2.0 Standard

Jeff Bake
Product Manager Engineer
DPSD Marketing
Intel Corporation

Overview

Intel is firmly committed to supporting the Universal Serial Bus (USB) 2.0 specification in future desktop board families by placing a discrete controller on the motherboard. USB 2.0, better known to consumers as "Hi-Speed USB," boosts the speed of peripheral-to-PC connections to 480 Mbps, or up to 40 times faster than USB 1.1 devices. It clearly enhances the bandwidth for the next generation of digital video, cameras, scanners, printers, hard drives, CDRWs, and DVD players.

Intel has supported USB 1.0 since its inception and is taking a leadership position again with Hi-Speed USB by contributing to the USB 2.0 specs and by designing the discrete solution for the desktop board. Intel is one of the first motherboard manufacturers to release products with USB 2.0 support.

In addition, Intel is working with Microsoft through the USB Implementers Forum (IF) to encourage compliance testing of USB 2.0 devices and drivers at plugfest events nationwide. The USB-IF maintains standards for USB peripherals. Approved devices are allowed to display an official USB logo.

Supports the Intel® Extended PC Concept

USB 2.0 supports Intel's Extended PC concept, which positions the PC as the center of a digitally connected peripheral world. It allows for higher bandwidth connections to take advantage of faster Intel processing power. Users will be able to connect DVD camcorders to their PCs and capture digital video to share with other PCs and devices wirelessly; they will be able to download images through digital cameras and scanners and share them. Figure 1 shows an internal block diagram of USB 2.0.

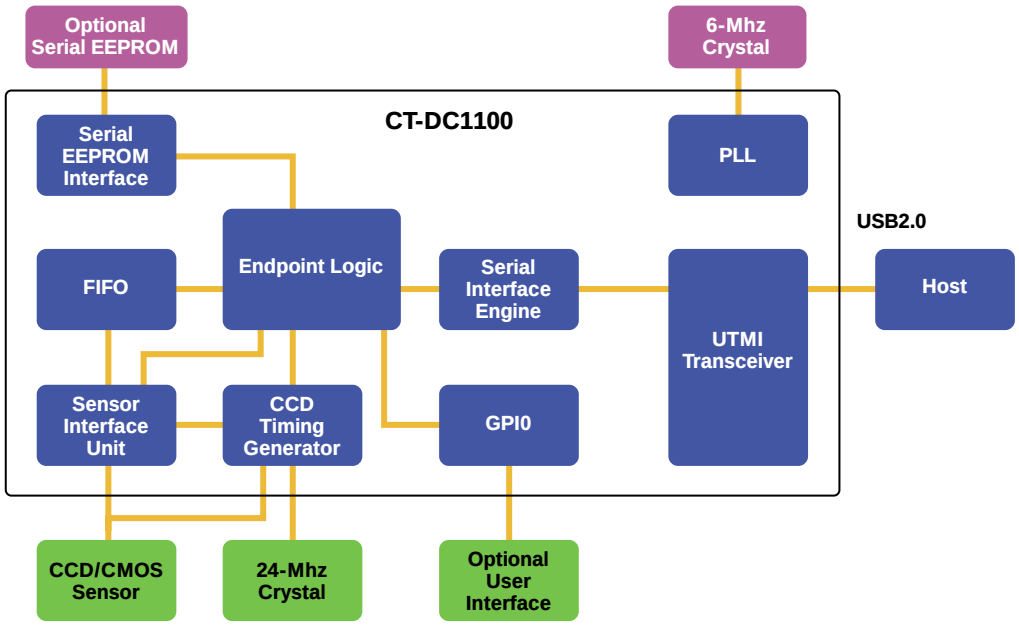

Figure 1. Internal Block Diagram of USB 2.0
Source: Cresentec Corporation

USB 2.0 Market Demand

According to a year 2000 study conducted by market analysts Cahners In-Stat Group, consumer spending on peripheral (Extended PC connection) devices external to the PC will accelerate. One Cahners In-Stat Group forecast calls for 47 million broadband homes to purchase 191 million digital devices between now and 2005–approximately 37 million in 2005 alone.

Superior Integration

Unlike most desktop board manufacturers, Intel integrates its USB 2.0 support on its motherboards. An additional benefit of having USB 2.0 on the board is to provide USB 2.0 routing to communication and networking riser (CNR). USB 2.0 provides bandwidth headroom for implementing current and future technologies such as Full Rate ADSL, Wireless 802.11b, and 802.11a through a CNR card.

Seamless Compatibility with USB 1.1

A user can plug any USB 1.1 device into any USB 2.0 port and obtain flawless operation; conversely, a USB 2.0 device will work in a USB 1.1 port, although much more slowly than the optimal 2.0 speed–480 Mbps. An additional benefit of USB 2.0 is that it uses the same cables and connectors as 1.1, thus eliminating any extra cost to upgrade to high-speed peripherals.

Microsoft Commitment to USB 2.0

Microsoft also supports the USB 2.0 standard. On April 23, 2001, the company sent a letter to customers from Carl Stork, general manager, MS Hardware Strategy, which said in part, “Microsoft is a big supporter of … USB 2.0 … as well as many other connection and wireless standards. We have been and remain committed to delivering support for these new standards in Windows* XP and some of our other operating system products.”

Summary

Intel has expressed its strong commitment to supporting the USB 2.0 standard in all its desktop boards. More popularly known as “Hi-Speed USB,” this peripheral standard is up to 40 times faster than the USB 1.0 standard, and it makes possible the use of high-bandwidth peripherals. This support is shared by other industry leaders, such as Microsoft.

More Info

For more information on the USB 2.0 standard, visit the Intel Developer site, the Everything USB site, and the USB Implementers Forum site.

Author Bio

Jeff Bake joined Intel in 1999 as product manager engineer for DPSD Marketing. Before coming to Intel, Jeff worked with an Internet start-up company that provided services and support to physicians and pharmaceutical companies via the Internet. He has also led market analysis efforts for a management consulting firm, and has developed and marketed practice management system software for a leading healthcare information systems company. Jeff earned his M.B.A. from Portland State University in 1993.

Initiatives and Technologies

Delivering Immersive Soccer Content to Sports Fans

Rajeeb Hazra
Senior Staff Engineer
Intel Architecture Labs
Intel Corporation

Overview

The traditional medium for delivering sports content to billions of fans around the world has been television. In recent years, the Internet has provided an additional avenue for delivering digital sports content to fans. Currently more than half of all online users use the Internet to look for sports information.

Until recently, the Internet experience for the fan has been limited to receiving textual information (with pictures and graphs) in addition to streaming and/or downloading audio and video. Today, immersive Internet applications are taking sports out of the mundane realm of passive viewing. Instead, cutting-edge technology, such as Intel's event modeling and event detection technologies, are helping sports events enter the realm of full interactive, personalized and customized viewing, virtual participation, and fantasy gaming.

The event model is a new form of sports media that provides a digital representation of a soccer game, for example. The soccer schema (game model) is written in the XML schema definition language (W3C recommendation, May 2, 2001) and can be mined extensively for interesting data. For example, developers can mine the synthesized game for on-demand video highlights, instant replays, immersive viewing (such as a specific player's point of view), user-defined custom statistics, active links, and coaching and training sequences and patterns.

Event Modeling

The event model itself is a digital playbook–a hierarchical representation of the game. Essentially, the event model is a representation of a conceptual model of the game. For example, every soccer game can be divided into two halves, plus an optional shootout. Each game segment can then be divided into a series of linked events, such as a pass, an assist, and a goal. Figure 1 shows how the set of properties (attributes) for a semantic entity relationship model can represent a goal event.

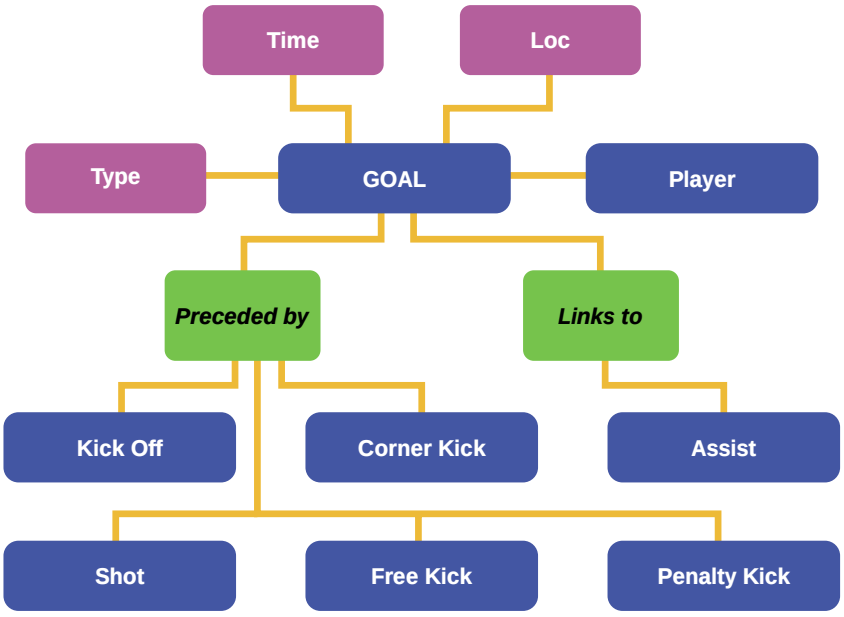

Figure 1. A semantic entity relationship model for goal event

The event model is expressed using a hierarchical entity relationship diagram. The entity relationship diagram is based on:

1. The laws that govern all soccer games
2. An understanding of how a soccer game progresses
3. All possible events that may happen during the course of a game

The event model is then transformed into an XML schema that is easy to mine, easy to describe tools in, and easy to parse. The conceptual model of the game becomes the source of prior domain knowledge for Intel's event detection algorithm.

Semantic Events

The creation of the event model for soccer starts with the process of tracking the players and other relevant game objects (such as the ball) for the duration of the game. The tracking data (positional information) can be generated in a number of ways using passive and/or active methods. Passive methods include video-based tracking; active methods include RF- and microwave-based tracking.

Once the positional information is available, the next step in creating the event model is to detect the significant events in the game. This step is performed using a combination of automatic event detection and manual input. For example, significant events in a soccer game include: ball out of bounds, corner kick, dead ball by ref, deflection, drop ball, free kick, foul, steal, and substitution. Significant actions include: defender movement (tackle), deflection, hug, kick, getting up, placing the ball on the ground, rolling, running, sliding, walking, and so on.

Traditional methods of event detection include manual, network-based, and rule-based event detection. These methods can detect selected types of events in various domains. However, they are inadequate for detecting the complete set of events in a given domain. They are also somewhat ad hoc and are not easily extensible, since they are tuned to a predefined set of events.

Intel's detection algorithm uses a rule-based methodology that can incorporate heuristics with rules of soccer. This rule-based architecture is hierarchical and extensible; that is, it doesn't prevent the use of other inference algorithms. Using the rule-based architecture, a game is evaluated so that the rules executed are only those rules relevant to the current situation. For example, Figure 2 shows a sample algorithm for a save event.

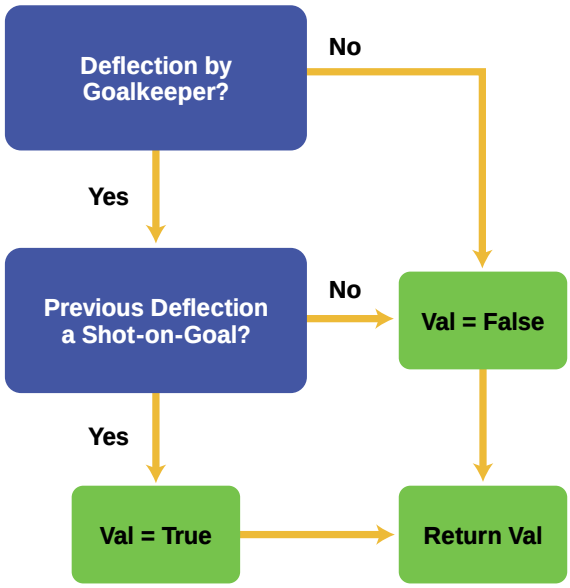

Figure 2. A sample save detection algorithm

Event Detection

Event detection occurs in two phases. Events detected in the second phase are more complex, based on the basic actions detected in the first phase.

- *First phase:* Computes the derived information (such as player motion and orientation) that is required by the rule-based algorithm, then identifies all sections of the tracking data that contain player-ball interactions. This includes eliminating all deflections of the ball (such as the ball bouncing off the ground), as opposed to deflections due to a player kick. Other factors in this phase include player proximity to the ball, the motion at the point of deflection (to see if force has been imparted to the ball), and so on.
- *Second phase:* Determines which rules from the domain knowledge base will be applied for each segment marked as a potential deflection by a player. It applies heuristic rules to detect the action that caused the event to occur. Then it uses the identified event to determine the next set of rules that will be evaluated to detect the next event.

Experiments have shown that Intel's event detection algorithm is significantly faster than real-time play. On average, Intel's algorithm takes less than one second to detect all actions and events in a 60-second game segment. The precision performance ranges from 93 percent to 96 percent for receptions and kicks to 100 percent precision for goals, save, and other events.

Summary

Intel has created a new class of real-time, data-streaming content for immersive sports viewing. This new digital medium enables developers to create new applications for content-based indexing and retrieval, data mining, automatic generation of statistics, electronic games, and coaching/training applications. This medium is extremely flexible and can be used for Internet, traditional broadcast, interactive TV, wireless services, and interactive sporting games. With immersive sports, league owners and other rights holders will see new licensing opportunities, while users will see personalized, customized, interactive sports as never before.

Intel, OradNet, AniVision, Virtual Spectator, Avid Sports, Sports Universal, and other companies are already offering or developing immersion sports applications. The next generation of applications will provide even more automation of event detection and will deal with multimodal input from both active and passive sensors. Although soccer is the current game of choice for applications, football, auto racing, sailing, and other sports are on the development table.

Experiments and current applications have already proven the speed and precision of Intel's event modeling and event detection technologies. Developers should begin applying Intel's leading-edge technologies now to take advantage of the many opportunities opening up in the realm of immersive sports.

More Info

Intel's white paper on immersive sports vision is available online at the Intel Labs site. Visit the Intel Architecture Labs Sports Immersion Web page to find out more information about sports immersion technologies and business trends, as well as white papers and articles.

A detailed description of the semantic event model, algorithms, and system architecture is offered in the technical paper "Detecting Semantic Events in Soccer Games: Towards a Complete Solution." The paper will be presented in August 2001 at the International Conference on Machine Learning (ICME) in Tokyo, Japan. The paper will be available online after the conference.

Intel® 3D software technologies, demos, and real-time solutions can be found in the 3D Software Technologies section of the Intel Architecture Labs area of the Intel Labs site.

Author Bio

Rajeeb Hazra is a senior staff engineer in the Intel Architecture Labs. He has worked on a variety of codecs and products, including Intel's VideoPhone® and ProShare® conferencing video codecs, Streaming Video Code, Sports Immersion, and Video-as-Input. Prior to joining Intel, Rajeeb worked at Lockheed Martin on advanced remote-sensing sensors and processing algorithms for NASA's Mission to Planet Earth program. He holds three patents, with 14 patents pending, and received the Intel Achievement Award in 2000. Rajeeb earned his M.S. and Ph.D. in computer science from the College of William and Mary.

Software

A Comprehensive Environment for Intel® IXP1200 Developers

Johnathan Corgan
Senior Product Line Manager
Intel Communications Group
Intel Corporation

Overview

Developers seeking a complete, cost-effective, and versatile way of rapidly creating next-generation applications for the Intel® IXP1200 Network Processor family now have a product tailor-made for their needs: the Intel® Internet Exchange Architecture (Intel® IXA) Software Developers Kit (SDK) 2.0.

In addition to providing system software for the IXP1200 family, the Intel IXA SDK 2.0 delivers an advanced, high-level programming framework and introduces support for the Linux* operating system alongside its existing support for VxWorks*. The SDK also includes a full suite of integrated development tools, robust API and infrastructure software mechanisms, and comprehensive building blocks and example code.

A number of innovative capabilities make the Intel IXA SDK 2.0 an ideal solution for network equipment developers designing for Internet edge and access customers in the enterprise and service-provider/metro market segments:

- *A Microengine C compiler* enables higher-level-language programming of microengine code for faster prototyping and reduced time-to-market.
- *A programming framework* enables the development of modular, portable code blocks and integration of third-party software products for more efficiently managing code modifications and upgrades.
- *A suite of example applications and software building blocks* simplifies initial development and upgrades alike.

Moreover, for helping to ensure compatibility, the Intel IXA SDK 2.0 retains and integrates all the features of the prior SDK (version 1.3), including ATM SAR and RFC1812 example code and IXP1200 C0 (Hyannis) hardware support.

Supports Microengine and StrongARM* Development

The Intel IXA SDK 2.0 provides IXP1200 developers a rich environment that includes tools for both the microengine and the StrongARM* code segments and supports both Linux and VxWorks embedded operating-system environments.

For simplified and portable microengine code development, the Intel IXA SDK 2.0 includes the brand-new Microengine C compiler as well as the IXP1200 Symbolic Language (microcode) assembler. Microengine C provides the ease of use of a higher-level language while offering the optimization abilities of a low-level language. The IXP1200 Symbolic Language enables microengine programming at any required level of abstraction and includes a large library of macros for simplified, optimized programming.

The primary environment for streamlining microengine development is the field-proven Intel IXA Developer's Workbench for the IXP1200 Network Processor. This graphical developer's environment features an advanced, thread-level, cycle-accurate, GUI-based simulator for the microengines and hardware interfaces, a packet generator that can simulate packet flow on the simulator, and a debugger with source-level capabilities for either the Microengine C or Symbolic Language compiler and usable on both the simulator and the target hardware.

For StrongARM code development, the SDK provides both Linux and VxWorks operating systems ported to the StrongARM core of the IXP1200 network processors along with development tools for each of them. Developers targeting Linux are provided GNU tools usable on either a Linux- or Windows NT*-based workstation using a command-line interface. The SDK also features an optional Windows NT-based IDE, which provides not only an interface for embedded-Linux application development but also capabilities for configuring, building, and debugging the Linux kernel itself.

Developers targeting VxWorks are provided a free evaluation copy of the Tornado* development environment from WindRiver Systems, including a C compiler and a debugger that connects to the target over a serial port or Ethernet (ships preinstalled on the IXDP1200 Advanced Development Platform). For both target platforms, the SDK provides Media Access Control (MAC) drivers for initializing devices on supported evaluation boards as well as drivers that allow packets to be passed from the microengine to the StrongARM core and from the line card to the host card. Also included are a Services Library for hash-unit and memory operations and the Hardware Abstraction Layer API.

Modular Programming Framework Enhances Portability

A central part of the Intel IXA SDK 2.0 is the Active Computing Element (ACE) programming framework. The framework provides a robust environment for encapsulating code blocks, either as common functions prewritten by Intel or original microcode, in a format that allows them to be easily coupled into complete packet-handling solutions. Once created, the ACE modules become portable building blocks for other applications.

Run-time support in the ACE framework includes a Resource Manager that manages various shared resources and enables developers to instantiate and load ACEs to microengines. The Resource Manager also supports the duplication of an ACE module and its resources on multiple microengines, simplifying the distribution and scaling of packet-processing functionality to parallel microengines and maximizing performance.

For defining ACE management interfaces, the SDK provides an interface description language allowing an ACE to be configured by application code or to communicate with other ACEs. In addition, a complete object management and communication infrastructure supports messaging through these interfaces and between the microengine- and StrongARM-based segments of the application.

The ACE framework and infrastructure also provide an ideal mechanism for integrating third-party software and Intel libraries, thereby simplifying code maintenance. Through this mechanism, third-party stacks, developer or third-party ACEs, and Intel® Library ACEs can be linked to the packet-processing pipeline and configured through well-defined interfaces. These ACEs can be easily swapped in and out or replaced with other ACEs developed in-house or purchased from third-party IXP1200 ecosystem developers.

Finally, to help developers and their customers to jump-start application development, the Intel IXA SDK 2.0 features a variety of powerful building blocks and example code.

- *For Linux developers*: ACEs for Layer 2 bridging, Layer 3 forwarding (RFC1812-compliant), NAT, and Filtering, and for processing ingress and egress data for two Intel® MAC chips, the IXF 440 (10/100 Ethernet) and IXF1002 (Gigabit Ethernet).
- *For VxWorks developers*: Complete applications performing Layer 2 bridging/filtering and Layer 3 forwarding for multiple port configurations as well as software for PPP-to-Ethernet protocol conversion and ATM SAR functions.

For Linux and VxWorks developers alike, the SDK also provides example code demonstrating various features of the languages, libraries, and underlying hardware.

Summary

The Intel Internet Exchange Architecture Software Developers Kit version 2.0 for the IXP1200 Network Processor (Intel IXA SDK 2.0) brings developers a total environment for simplifying and accelerating development of IXP1200 designs. The Intel IXA SDK 2.0 provides IXP1200 system software, an advanced, high-level programming framework, and full suite of integrated development tools, robust API and infrastructure software mechanisms, and comprehensive building blocks and example code. The Intel IXA SDK 2.0 also fully supports developers targeting both Linux and VxWorks embedded operating systems.

The Intel IXA SDK 2.0 is available in beta release June 2001 and in production release later in Q3. Both the Microengine C compiler and the Embedded Linux IDE are provided on the IXA SDK 2.0 CD as free 60-day evaluation copies. Keys for these optional tools may be purchased on the Intel Developer Web site in Q3.

The IXA SDK 2.0 will ship with the IXDP1200 Advanced Development Platform or you may order a copy from the Intel Developer Web site.

More Info

For more on the Intel Internet Exchange Architecture Software Developers Kit 2.0 for the IXP1200 Network Processor, including ordering information, visit the IXA SDK 2.0 Web site.

For information about the Intel Internet Exchange Architecture, visit the Intel IXA Web site.

Information about Intel® networking and communications technologies and products is available from the Networking and Communications Building Blocks area of the Intel Developer Web site.

Author Bio

Johnathan Corgan is a senior product line manager in the Network Processor Business Unit. Before joining Intel in early 2000, he served as director of product management for VPNet Technologies and as product line manager for VPN Systems at 3Com Corporation.

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